CLAIMS

Listing of claims:

1. (Previously Presented) A system comprising:

a general purpose DMA controller, the general purpose DMA controller being configured to control a plurality of different types of DMA transfers between a plurality of different combinations of a plurality of different types of hardware resources;

an arithmetic circuit, the arithmetic circuit being coupled to receive data from the general purpose DMA controller, the arithmetic circuit generating an error checking value based on the data received from the general purpose DMA controller and based on a polynomial equation; and

wherein the arithmetic circuit is capable of being programmed with a plurality of different polynomial equations usable to generate error checking values of different types~~.~~ and wherein the arithmetic circuit is a linear feedback shift register wherein the linear feedback shift register includes a plurality of feedback points, the feedback points determining the form of a polynomial that is used in the polynomial equation, and wherein the feedback points are programmable.

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2. (Canceled)

3. (Canceled)

4. (Original) A system according to claim 3, wherein the linear feedback shift register comprises a plurality of the multiplexers, and wherein each multiplexer is programmable to determine whether a polynomial in the polynomial equation has a particular exponential term.

5. (Original) A system according to claim 4, wherein the system further comprises a programmable shift register, the programmable shift register being programmable to shift different block sizes of data into the linear feedback shift register.

6. (Original) A system according to claim 5, wherein the linear feedback shift register is capable of being programmed with divisor polynomials having each of the following forms: $x^{16} + x^{15} + x^2 + 1$; $x^{16} + x^{14} + x + 1$; $x^{16} + x^{12} + x^5 + 1$; $x^{16} + x^{11} + x^4 + 1$; and $x^{32} + x^{26} + x^{23}\, x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$.

7. (Original) A system according to claim 1, wherein the arithmetic circuit performs polynomial division, and wherein the divisor polynomial is programmable.

8. (Original) A system according to claim 1, wherein the error checking value is a cyclic redundancy check value.

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9. (Original) A system according to claim 1, wherein the polynomial equation includes a polynomial with a plurality of exponential terms, and wherein the system further comprises a polynomial register comprising a plurality of bits, each bit determining whether a particular exponential term is present in the polynomial of the polynomial equation.

10. (Original) A system according to claim 1, wherein the general purpose DMA controller is capable of controlling DMA communication of data from a universal asynchronous transmitter-receiver, a memory controller, and a serial port interface.

11. (Original) A system comprising:
    (A) a general purpose DMA controller;
    (B) a linear feedback shift register, the linear feedback shift register being coupled to receive data from the general purpose DMA controller, the linear feedback shift register comprising a plurality of programmable polynomial building blocks, the plurality of programmable polynomial building blocks being connected in a sequence with each building block corresponding to a respective exponential term in a polynomial of a polynomial equation implemented by the linear feedback shift register, each building block comprising
        (1) a feedback gate, the feedback gate being coupled to an output of an adjacent polynomial building block in the sequence and to a non-adjacent polynomial building block in the sequence,
        (2) a multiplexer, the multiplexer being coupled to an output of the feedback gate and to the output of the adjacent polynomial building block in the sequence, the multiplexer determining whether the flip flop receives an input from an output of the feedback gate or from the output of the adjacent polynomial building block,
        (3) a flip flop, the flip flop having an input coupled to an output of the multiplexer, and

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wherein, when the flip flop receives an input from the output of the feedback gate, the respective exponential term is included in the polynomial,

wherein, when the flip flop receives an input from the immediately-preceding flip flop, the respective exponential term is not included in the polynomial, and

wherein the multiplexers of each of the programmable polynomial building blocks are programmable to determine which of the exponential terms are included in the polynomial of the polynomial equation.

12. (Original) A system according to claim 11, wherein the linear feedback shift register performs polynomial division, and wherein the polynomial is a polynomial divisor.

13. (Original) A system according to claim 11, wherein the system further comprises a polynomial register comprising a plurality of bits, each bit determining whether a particular exponential term is present in the polynomial of the polynomial equation.

14. (Original) A system according to claim 11, wherein the system further comprises a programmable shift register, the programmable shift register being programmable to shift different block sizes of data into the linear feedback shift register.

15. (Original) A system according to claim 11, wherein the general purpose DMA controller is capable of controlling DMA communication of data from a universal asynchronous transmitter-receiver, a memory controller, and a serial port interface.

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16. (Original) A circuit according to claim 11, wherein the feedback gate is an XOR gate.

17. (Original) A system according to claim 11, wherein the linear feedback shift register is capable of being programmed with a divisor polynomial having the following form: $x^{16} + x^{15} + x^2 + 1$.

18. (Original) A system according to claim 11, wherein the linear feedback shift register is capable of being programmed with a divisor polynomial having the following form: $x^{16} + x^{12} + x^5 + 1$.

19. (Original) A system according to claim 11, wherein the linear feedback shift register is capable of being programmed with a divisor polynomial having the following form: $x^{16} + x^{11} + x^4 + 1$.

20. (Original) A system according to claim 11, wherein the lincar feedback sh& register is capable of being programmed with a divisor polynomial having the following form: $x^{32} + x^{26} + x^{23} x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x + 1$.

21. (Original) A system according to claim 1 1, wherein the linear feedback shift register is capable of being programmed with divisor polynomials having each of the following forms: $x^{16} + x^{15} + x^{2} + 1$; $x^{16} + x^{14} + x + 1$; $x^{16} + x^{12} + x^{5} + 1$; $x^{16} + x^{11} + x^{4} + 1$; and $x^{32} + x^{26} + x^{23} x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x + 1$

22. (Previously Presented) A system comprising:

a plurality of different types of hardware resources;

a plurality of general purpose DMA controllers, the plurality of general purpose DMA controllers being coupled to respective ones of the plurality of hardware resources, the coupling of the general purpose DMA controllers to the plurality of hardware resources being programmable, such that each of the general purpose DMA controllers may be programmably coupled to different ones of the plurality of different hardware resources, the plurality of general purpose DMA controllers each being configured to control a plurality of different types of DMA transfers between a plurality of different combinations of the plurality of different types of hardware resources;

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a plurality of arithmetic circuits, the plurality of arithmetic circuits being coupled to respective ones of the plurality of general purpose DMA controllers, each of the plurality of arithmetic circuits being coupled to receive data from the respective general purpose DMA controller, and each of the plurality of the arithmetic circuits generating an error checking value based on the data received from the respective general purpose DMA controller and based on a polynomial equation; and

wherein each of the plurality of arithmetic circuits is capable of being programmed with a plurality of different polynomial equations usable to generate error checking values of different types.

23. (Previously Presented) A system according to claim 22, wherein each of the plurality of arithmetic circuits is capable of being programmed with divisor polynomials having each of the following forms: $x^{16} + x^{15} + x^2 + 1$; $x^{16} + x^{14} + x + 1$; $x^{16} + x^{12} + x^5 + 1$; $x^{16} + x^{11} + x^4 + 1$; and $x^{32} + x^{26} + x^{23} x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$.

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